Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1.-5. (canceled)

C1

Claim 6. (previously presented) A wafer for use in making a chip device, the wafer comprising:

a non-passivated die;

a first titanium layer at non-isolation locations on the die;

a first copper layer directly on the first titanium layer;

a titanium passivation layer directly on the first copper layer at non-solder bump locations; and

under bump material directly on the first copper layer at solder bump locations.

Claim 7. (currently amended) A wafer in accordance with claim 6 further comprising a solder bump ~~bumps~~ on the under bump material.

Claim 8. (previously presented) A chip device comprising:

a non-passivated die;

a first titanium layer at non-isolation locations on the die;

a first copper layer directly on the first titanium layer;

a titanium passivation layer directly on the first copper layer at non-solder bump locations; and

under bump material directly on the first copper layer at solder bump locations.

Claim 9. (currently amended) A chip device in accordance with claim 8 further comprising a solder bump ~~bumps~~ on the under bump material.

Claim 10. (new) A chip device comprising:

a non-passivated die;

a first titanium layer on the non-passivated die;

a copper layer directly on the first titanium layer;

a second titanium layer directly on the copper layer, wherein the second titanium layer includes an aperture;

a copper structure within the aperture of the second titanium layer; and

a solder structure over the copper structure.

Claim 11. (new) The chip device of claim 10 wherein the solder structure is a solder ball.

Claim 12. (new) The chip device of claim 10 wherein the first titanium layer, the copper layer, the second titanium layer, the copper structure, and the solder structure are at non-isolation locations of the non-passivated die.